

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: ) Art Unit:  
 Chintan Desai ) Examiner:  
 Serial No. [Not yet assigned] )  
 Filed: December 21, 1999 )  
 For: RECEIVER DESERIALIZER )  
 CIRCUIT FOR FRAMING PARALLEL )  
 DATA )

jc530 U.S. PTO  
 09/468746  
 12/21/99

**CERTIFICATE OF MAILING**

"Express Mail" mailing label no: EL100016184US

Date of Deposit: December 21, 1999

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR

1.10 on the date indicated above and is addressed to:

Box Patent Application

Assistant Commissioner for Patents

Washington, D.C. 20231

  
 Diane Morse

**TRANSMITTAL LETTER**

Honorable Assistant Commissioner  
 for Patents  
 Box Patent Application  
 Washington, D.C. 20231

Dear Sir:

Enclosed for filing please find the patent application for an invention entitled, "RECEIVER DESERIALIZER CIRCUIT FOR FRAMING PARALLEL DATA", filed on behalf of LSI Logic Corporation, assignee from inventor Chintan Desai, including Utility Patent Application Transmittal, 12 pages of specification, 5 pages of claims, 5 sheets of drawing figures, and 1 page of Abstract. Also enclosed herewith are the Combined Declaration and Power of Attorney, and Recordation Form Cover Sheet and Assignment.

The attorney's Docket Number is LSI-99-299.

Kindly address all communications regarding this application to:

Bruce R. Hoppenfeld  
LSI Logic Corporation  
Patent Law Department  
1551 McCarthy Boulevard, M/S D-106  
Milpitas, CA 95035

A check in the amount of \$760.00 is enclosed for the filing fee for a large entity, calculated as follows:

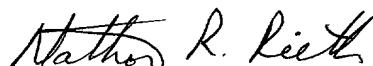
Basic Filing Fee:	\$ 760.00
No Additional Independent Claims:	\$ .00
20 Additional Dependent Claims	\$ .00
No <u>Multiple Dependent Claims:</u>	\$ .00
Total Filing Fee:	\$ 760.00

A check in the amount of \$40.00 is also enclosed for the Assignment fee.

In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, the Assistant Commissioner is hereby authorized to charge or credit the difference to our Deposit Account No. 04-0025. A duplicate of this page is enclosed.

Respectfully submitted,  
D'ALESSANDRO & RITCHIE

Dated: December 21, 1999

  
Nathan R. Rieth  
Reg. No. 44,302

D'Alessandro & Ritchie  
P.O. Box 640640  
San Jose, CA 95164-0640  
(408) 441-1100


Please type a plus sign (+) inside this box → ☒


PTO/SB/05 (4/98)  
Approved for use through 09/30/2000. OMB 0851-0032  
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE  
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	ISI-99-299
First Inventor or Application Identifier	Chintan Desai
Title	Receiver Deserializer Circuit For ...
Express Mail Label No.	EL100016184US

<b>APPLICATION ELEMENTS</b> See MPEP chapter 600 concerning utility patent application contents.		<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. <input checked="" type="checkbox"/> Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)		5. <input type="checkbox"/> Microfiche Computer Program (Appendix)	
2. <input checked="" type="checkbox"/> Specification [Total Pages 18] (preferred arrangement set forth below) - Descriptive title of the invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the invention - Brief Summary of the invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure		6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies	
3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 5]		<b>ACCOMPANYING APPLICATION PARTS</b>	
4. Oath or Declaration [Total Pages 2] a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed) i. <input type="checkbox"/> <b>DELETION OF INVENTOR(S)</b> Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).		7. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s)) 8. <input type="checkbox"/> 37 C.F.R. § 3.73(b) Statement <input checked="" type="checkbox"/> Power of Attorney (when there is an assignee) 9. <input type="checkbox"/> English Translation Document (if applicable) 10. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations 11. <input type="checkbox"/> Preliminary Amendment 12. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) (Should be specifically itemized) * Small Entity <input type="checkbox"/> Statement filed in prior application, Status still proper and desired (PTO/SB/09-12) 13. <input type="checkbox"/> Statement(s) 14. <input type="checkbox"/> Certified Copy of Priority Document(s) (if foreign priority is claimed) 15. <input type="checkbox"/> Other:	
<b>NOTE FOR ITEMS 1 &amp; 15: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).</b>			
16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment: <input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input type="checkbox"/> Continuation-in-part (CIP) of prior application No: _____ Prior application information: Examiner _____ Group / Art Unit: _____ For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.			
<b>17. CORRESPONDENCE ADDRESS</b>			
<input type="checkbox"/> Customer Number or Bar Code Label  or <input type="checkbox"/> Correspondence address below (Insert Customer No. or Attach bar code label here)			
Name	Bruce R. Hoppenfeld		
Address	ISI Logic Corporation, Patent Law Department 1551 McCarthy Boulevard		
City	Milpitas	State	CA
Zip Code	95035		
Country	USA	Telephone	408-433-6100
Fax	408-433-7770		

Name (Print/Type)	Nathan R. Rieth	Registration No. (Attorney/Agent)	44,302
Signature		Date	12/21/99

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

5

TITLE OF INVENTION

## 10

## Field of the Invention

## Background

1

word has been lost in its transmission. The result is incorrectly framed parallel data words at the receiver which contain some bits belonging to the previous eight bit word or which contain some bits belonging to the next eight bit word.

5        This framing process is demonstrated generally in **FIG. 1**, which depicts a block diagram of a typical receiver deserializer along with a timing diagram showing how the received serial data is framed into parallel words based on a word clock. A sampling flip flop **100** receives serial data and retimes it with the rising edge of a recovered clock. The recovered clock is the source of eight phases  
 10        generated by a clock generator **104**. The serial data is sampled by the eight phases to generate eight bits. The eight bits are finally re-timed on one of the phases, channel word clock, to form a parallel data word. With bits B<sub>7</sub>-B<sub>0</sub> making up the original parallel word which was serially transmitted, the timing diagram of **FIG. 1** illustrates how in a typical deserializer, the received data can be incorrectly  
 15        framed as a parallel data word.

Prior methods for solving this problem include the use of additional storage elements to store the last received eight bit word in order to create a new sixteen bit word from the last word and the current word. A block diagram of a  
 20        deserializer which implements this prior method is shown in **FIG. 2**. An array of eight storage flip flops **200** is used to store a previously received eight bit word which is then combined with a currently received eight bit word. The new sixteen

bit word contains a predefined data reference pattern which is transmitted upon initialization of the circuit. A comparator **202** searches through the new sixteen bit word for the predefined reference pattern and identifies the pattern location to a sixteen-to-eight multiplexer **204**. The sixteen-to-eight multiplexer **204** then selects  
5 these bits as the correct eight bits to be framed with word clock and output as received data.

The timing diagram of **FIG. 3** further illustrates this prior method for framing parallel data as implemented by the circuit of **FIG. 2**. Where bits  $B_7$ - $B_0$   
10 represent an eight bit predefined reference pattern, the diagram indicates the combination of current and last data which forms a sixteen bit data word containing this predefined reference pattern. The bit locations of the predefined reference pattern within the sixteen bit data word are found through multiple comparisons made by the comparator **202** of **FIG. 2**. Once located by the  
15 comparator **202**, these bit locations are selected by the multiplexer **204** as containing the correct eight bits to be framed with word clock and output as received data.

This and other prior methods of framing parallel data can present  
20 significant costs in time and materials when implementing. For example, it is apparent from the timing diagram of **FIG. 3** that framing parallel data by the method presented in **FIG. 2**, introduces unwanted latency. There is a necessary

penalty of one word clock associated with the prior method of forming a sixteen bit data word to locate the predefined eight bit reference pattern.

Additionally, increased scrutiny of the block diagram circuit of **FIG. 2** indicates the complexity of the circuitry required to implement this prior method, as illustrated in **FIG. 4**. A circuit framework for the multiplexer **204** and comparator **202** blocks of **FIG. 2** is presented in **FIG. 4**. Though not intended as a complete representation of these circuit blocks, the depiction in **FIG. 4** shows the significant hardware required to implement the comparator **202** block of **FIG. 2**. Nine different sets of bit locations exist within the sixteen bit word where the predefined eight bit reference pattern might be encountered. For example, the predefined eight bit reference pattern could be located in bit locations 0-7, 1-8, 2-9, 3-10, 4-11, 5-12, 6-13, 7-14, or 8-15. It is therefore necessary to dedicate nine sets of eight comparators each to search these locations in order that the multiplexer **204** can select the correct location for framing the parallel data.

The disadvantages apparent in this and other prior methods of framing parallel data can therefore include requirements for additional data storage elements, complex comparator and multiplexer circuits, and unwanted latency inherent to these methods.

Accordingly, there exists a need for an efficient, simple and low latency method for framing the parallel data generated by a receive deserializer circuit.



## SUMMARY OF THE INVENTION

A receive deserializer circuit which frames parallel data utilizes a skip-bit technique for aligning a predefined data reference pattern with a word clock. The receive deserializer circuit includes a sampling flip flop which receives serial data including a data reference pattern. The sampling flip flop samples and retimes the serial data to a recovered clock. A demultiplexer then deserializes the retimed serial data into a parallel data word which is timed to a word clock from a clock generator. A comparator makes comparisons of the parallel data word with a preset data reference pattern until a match results. A logic controller interprets whether the output of the comparator is a match and generates a shift pulse following each comparison which does not result in a match. The clock generator divides the recovered clock into eight phase clocks. One of the phase clocks is a word clock. Each time the clock generator receives a shift pulse from the logic controller, it disables all the phase clocks by one bit period. This results in a one bit shift in all the clocks and a one bit shift in the parallel data generated on word clock each time there is no match from the comparator. When a match occurs, no shift pulse is generated by the logic controller, and the predefined data reference pattern and subsequent data words are properly framed on the word clock.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block and timing diagram of a typical deserializer in accordance with the prior art illustrating a loss of word boundary information upon data transmission.

FIG. 2 is a block diagram of a deserializer circuit in accordance with the prior art illustrating a method for framing parallel data using additional storage elements.

FIG. 3 is a timing diagram illustrating the method for framing parallel data of the deserializer circuit of FIG. 2 in accordance with the prior art.

FIG. 4 is a diagram of the multiplexer and comparator portions of the deserializer circuit of FIG. 2 in accordance with the prior art, illustrating the complexity of implementing the comparator.

FIG. 5 is a block diagram of the deserializer circuit in accordance with a preferred embodiment of the present invention.

FIG. 6 is a diagram of the individual comparators within the comparator block of FIG. 5 in accordance with a preferred embodiment of the present invention.

FIG. 7 is a timing diagram illustrating the method for framing parallel data of the deserializer circuit of FIG. 5 in accordance with a preferred embodiment of the  
5 present invention.

## DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons after a perusal of this disclosure.

A preferred embodiment of the present invention is illustrated in the block diagram schematic of **FIG. 5**. In this illustration, control logic **500** is incorporated into a receive deserializer circuit similar to the circuit shown by the prior art of **FIG. 2**. The control logic **500** initiates the skip-bit framing method of the present invention which eliminates the need for additional flip flop storage elements **200**, complex comparators **202**, and sixteen-to-eight multiplexers **204** as illustrated in the prior art of **FIG.'s 2 & 4**.

The receive deserializer circuit of **FIG. 5** comprises a sampling flip flop **502** which receives serial data from a transmitter circuit (not shown). The serial data includes a data reference pattern which is transmitted from the transmitter upon initialization of the circuit. The data reference pattern is typically, but not necessarily, an eight bit word. The sampling flip flop **502** retimes the serial data to a recovered clock. The recovered clock is a clock which is local to the receiver circuit and which has been aligned on its negative edge with the transition edge of the incoming serial data by a clock recovery module (not shown).

A clock generator **506** divides down the recovered clock and generates eight phase clocks at a frequency eight times slower than the recovered clock. One of the phase clocks is word clock. The serial retimed data is sampled by each phase clock to generate eight bits which are retimed with word clock as parallel data by a demultiplier **504**. In general, the parallel data word is compared by a comparator **508** which searches for the data reference pattern transmitted from the transmitter upon initialization of the circuit. The control logic **500** interprets whether the output of the comparator is a match and generates a shift pulse following each comparison which does not result in a match. When the clock generator **506** receives the shift pulse, it disables all the phase clocks by one bit period. This results in a one bit shift in the clocks with respect to the serial data and a one bit shift in the parallel data generated on word clock. Once the parallel data word contains all bits of the predefined data reference pattern, no shift pulse will be generated by the control logic **500**, and the parallel data word and all subsequent data words are properly framed on the word clock.

More specifically, a set of individual comparators **600** as shown in **FIG. 6** make up the comparator **508** of **FIG. 5**. The number of individual comparators **600** is typically eight, but in any event will be equal to the number of bits in the data reference pattern. The individual comparators **600** are typically operational amplifiers or logic gates such as exclusive OR gates. Each individual comparator

600 as shown in FIG. 6, has a first input tied to a preset bit representing a bit from the known data reference pattern. This preset bit is typically hardwired as an input to the individual comparator 600, but could also be set upon initializing the receive deserializer circuit and stored in a storage element which then acts as the first

5 input to an individual comparator 600. The second input to each individual comparator 600 is a corresponding bit from the parallel data word deserialized by the demultiplexer 504 of FIG. 5. The individual comparators 600 indicate a match when the preset bit and the corresponding bit from the parallel data word are the same. The control logic 500 effectively ANDs the individual comparator

10 600 outputs together to determine if there has been a match between all the preset bits and all the bits in the parallel data word. If all the individual comparators 600 do not indicate a match at the same time, the control logic 500 generates a shift pulse to the clock generator 506 as indicated in FIG. 5. If all the individual comparators 600 indicate a match at the same time, the control logic 500 does not

15 generate a shift pulse, and the parallel data word is then known to contain the data reference pattern, which has thus been properly framed. The subsequent serial data being received on word clock is therefore also properly framed.

In addition to the demonstrated benefits of a reduced need for flip flop

20 storage elements, complex comparators, and sixteen-to-eight multiplexers, the timing diagram as shown in FIG. 7 also illustrates the benefit of reduced latency that is gained by the framing method of the present invention. From the timing

diagram of **FIG. 7** it is apparent that if the word boundary and word clock is skewed by one bit period, the additional latency will only be one bit period. Furthermore, the maximum latency that can be generated by the framing method of the present invention as illustrated in **FIG.'s 5 & 7**, is four bit periods since the word clock can be effectively shifted in either direction with respect to the sampled serial data and it can never be skewed more than four bit periods away from one of the word boundaries of an eight bit word. By contrast, the latency introduced by the prior art method as shown in the timing diagram of **FIG. 3** will always be one word clock cycle, regardless of the amount of initial skew in the word clock and word boundary.

#### Alternative Embodiments

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

## CLAIMS

What is claimed is:

1. A receive deserializer circuit which frames data, comprising:

a sampling flip flop for receiving serial data including a data reference  
 5 pattern, wherein said sampling flip flop retimes said serial data to a recovered  
 clock as sampled serial data;

a demultiplexer for deserializing said sampled serial data into a parallel data  
 word timed to a word clock from a clock generator;

a comparator for making a comparison of said parallel data word with a  
 10 preset data reference pattern until said comparison results in a match;

a logic controller for interpreting whether the output of said comparator  
 results in said match and for generating a shift pulse following each of said  
 comparisons which do not result in said match; and

said clock generator for dividing said recovered clock into phase clocks,  
 15 said word clock being one of said phase clocks, and for disabling said phase  
 clocks for a period of one bit upon receipt of said shift pulse, thereby creating a  
 one bit shift in the alignment of said parallel data word being generated on said  
 word clock by said demultiplexer.



2. The circuit as recited in claim 1, wherein said recovered clock is a local clock whose negative edge is pre-aligned with the transition edge of said serial data by a clock recovery module.

5 3. The circuit as recited in claim 1, wherein said recovered clock is the source clock for said phase clocks.

4. The circuit as recited in claim 1, wherein said preset data reference pattern is derived from a plurality of hard-wired connections.

10

5. The circuit as recited in claim 1, wherein said preset data reference pattern is derived from data received from a transmitter upon initialization of said circuit.

15

6. The circuit as recited in claim 1, wherein said comparator is a plurality of comparators whose outputs are combined by said logic controller to determine whether said comparator results in said match.

20

7. The circuit as recited in claim 6, wherein each of said plurality of comparators has a first and second input, said first input driven by a separate reference bit from said preset data reference pattern and said second input driven by a separate sample bit from said parallel data word.

8. The circuit as recited in claim 6, wherein said plurality of comparators is selected from the group consisting of operational amplifiers, logic gates and combinations thereof.

5 9. The circuit as recited in claim 6, wherein said plurality of comparators is eight exclusive OR logic gates.

10. A method of framing data in a receive deserializer circuit, comprising the steps of:

10 receiving serial data including a data reference pattern from a transmitter;  
 retiming said serial data to a recovered clock as sampled serial data;  
 deserializing said sampled serial data into a parallel data word timed to a  
 word clock;  
 comparing said parallel data word with a preset data reference pattern until  
 15 a match results;  
 generating a shift pulse when said comparing does not result in said match;  
 dividing said recovered clock into phase clocks, including said word clock;  
 and  
 disabling said phase clocks for one bit period each time said shift pulse is  
 20 generated, thereby creating a one bit shift in the alignment of said parallel data  
 word being generated on said word clock in said demultiplexer.

11. The method as recited in claim 10, wherein said recovered clock is a local clock whose negative edge is pre-aligned with the transition edge of said serial data by a clock recovery module.

5 12. The method as recited in claim 10, wherein said recovered clock is the source clock for said phase clocks.

13. The method as recited in claim 10, wherein said preset data reference pattern is derived from a plurality of hard-wired connections.

10

14. The method as recited in claim 10, wherein said preset data reference pattern is derived from data received from a transmitter upon initialization of said receive deserializer circuit.

15 15. The method as recited in claim 10, wherein said comparator is a plurality of comparators whose outputs are combined by said logic controller to determine whether said comparator results in said match.

16. The method as recited in claim 15, wherein each of said plurality of  
20 comparators has a first and second input, said first input driven by a separate reference bit from said preset data reference pattern and said second input driven by a separate sample bit from said parallel data word.

17. The method as recited in claim 15, wherein said plurality of comparators is selected from the group consisting of operational amplifiers, logic gates and combinations thereof.

5

18. The method as recited in claim 15, wherein said plurality of comparators is eight exclusive OR logic gates.

19. A method of framing data in a receive deserializer circuit, comprising the  
10 steps of:

receiving serial data;

generating a local clock based on said serial data;

deserializing said serial data into a parallel data word;

comparing a portion of said parallel data word with a preset data reference

15 pattern;

adjusting said local clock to an adjusted local clock based on the results of  
said comparing; and

timing subsequent data to said adjusted local clock.

ABSTRACT OF THE DISCLOSURE

A receive deserializer circuit which frames parallel data utilizes a skip-bit technique for aligning a predefined data reference pattern with a word clock. The receive deserializer circuit includes a sampling flip flop which receives serial data including a data reference pattern. The sampling flip flop samples and retimes the serial data to a recovered clock. A demultiplexer then deserializes the retimed serial data into a parallel data word which is timed to a word clock from a clock generator. A comparator makes comparisons of the parallel data word with a preset data reference pattern until a match results. A logic controller interprets whether the output of the comparator is a match and generates a shift pulse following each comparison which does not result in a match. The clock generator divides the recovered clock into eight phase clocks. One of the phase clocks is a word clock. Each time the clock generator receives a shift pulse from the logic controller, it disables all the phase clocks by one bit period. This results in a one bit shift in all the clocks and a one bit shift in the parallel data generated on word clock each time there is no match from the comparator. When a match occurs, no shift pulse is generated by the logic controller, and the predefined data reference pattern and subsequent data words received on word clock are properly framed.

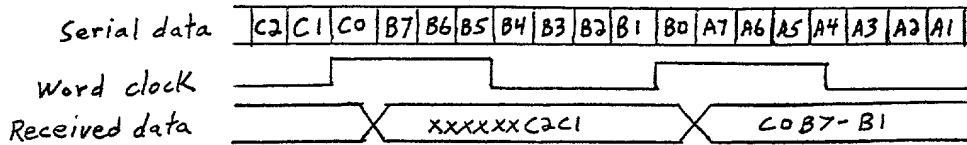
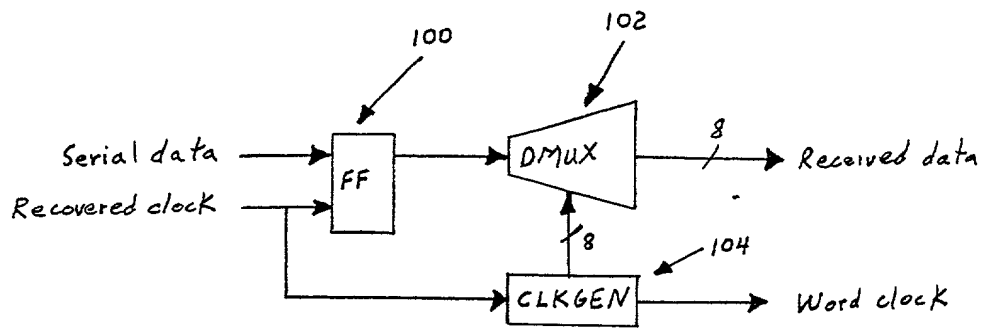


FIG. 1

PRIOR ART

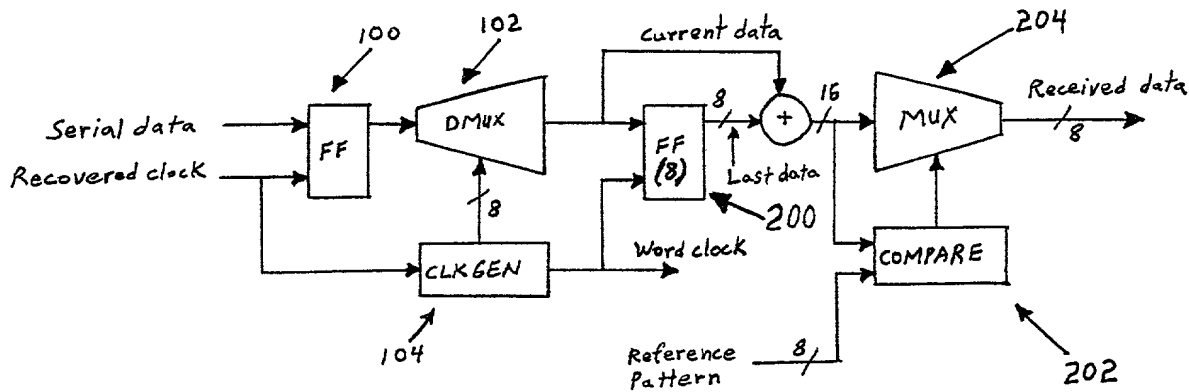
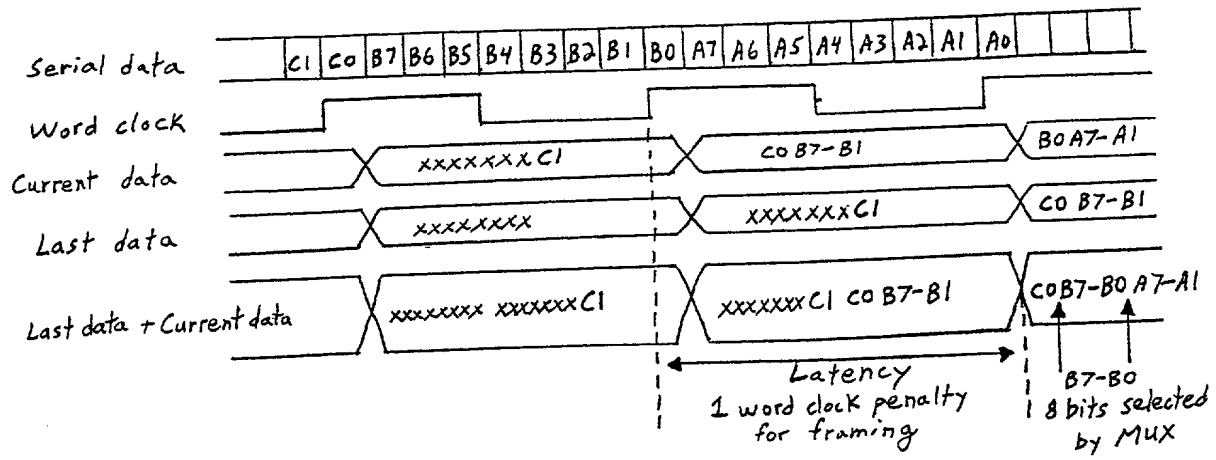
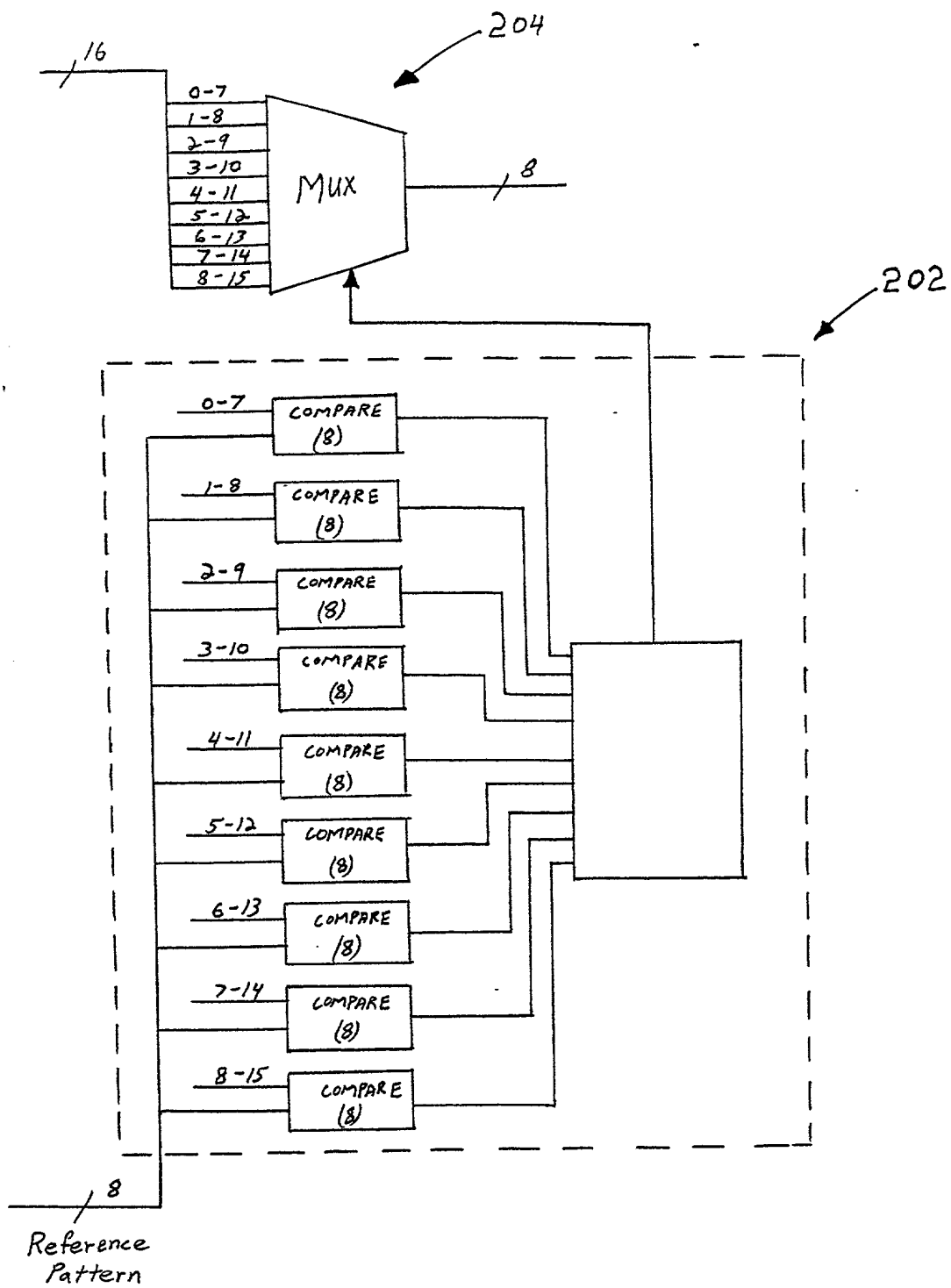


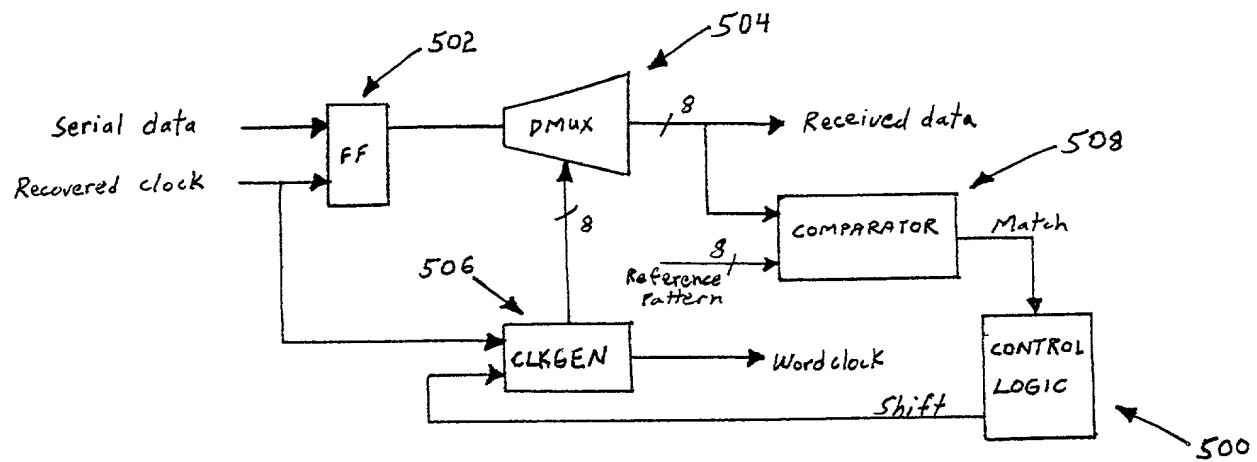
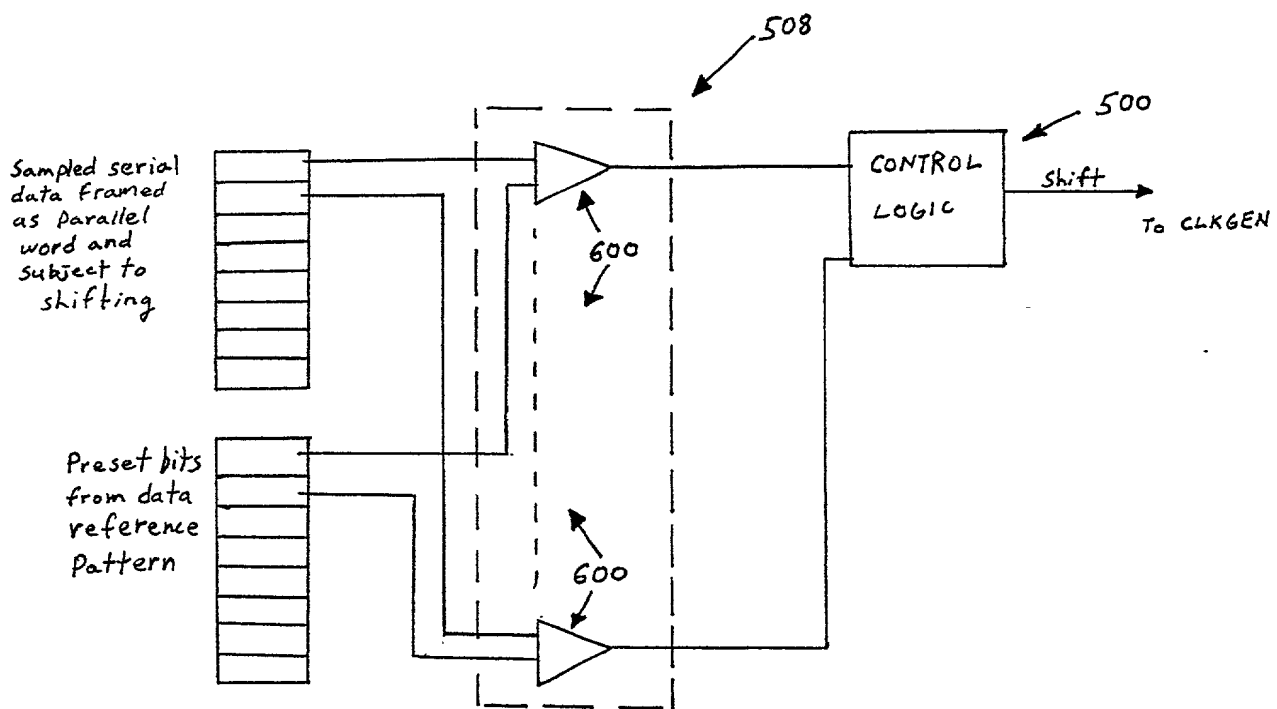
FIG. 2

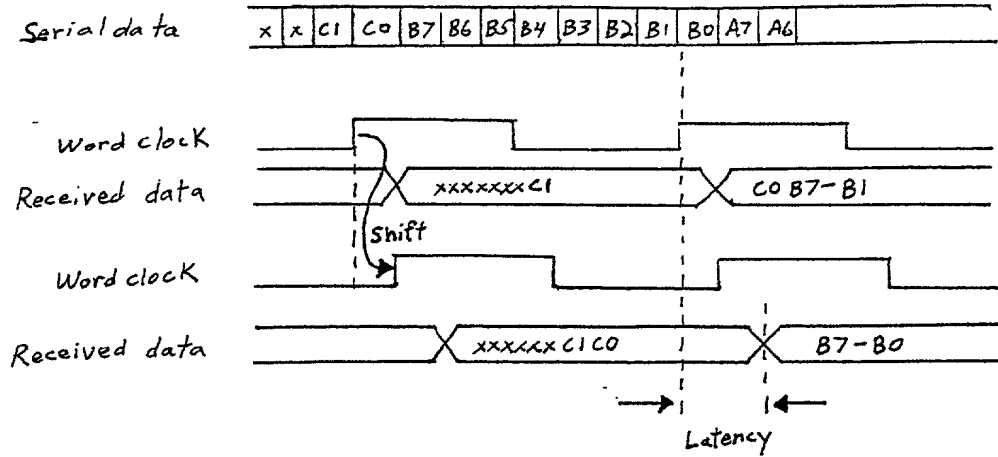
PRIOR ART

FIG. 3PRIOR ART

FIG. 4PRIOR ART



FIG. 5FIG. 6

FIG. 7

## COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: RECEIVE DESERIALIZER CIRCUIT FOR FRAMING PARALLEL DATA, the specification of which

  X   is attached hereto;  
       was filed on xxxxxx as application serial no. xxxxxx;  
       was amended on xxxxxx.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority
(Serial No.)	(Country)	(Filing Date)	Yes ___ No ___
(Serial No.)	(Country)	(Filing Date)	Yes ___ No ___

I hereby claim the benefit under Title 35, United States Code, Sec. 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Sec. 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Serial No.)	(Filing Date)	(Status)
(Serial No.)	(Filing Date)	(Status)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark office connected therewith:

David G. Pursel, Reg. No. 28,659; Ralph R. Veseli, Reg. No. 33,807; Bruce R. Hopenfeld, Reg. No. 39,714; Sandeep Jaggi, Reg. No. 43,331; Gary Edward Ross, Reg. No. 29,431; Kenneth D'Alessandro, Reg. No. 29,144; David B. Ritchie, Reg. No. 31,562; Marc S. Hanish, Reg. No. 42,626; John P. Schaub, Reg. No. 42,125; Gerhard W. Thielman, Reg. No. 43,186; Reynaldo C. Barceló, Reg. No. 42,290; Lee M. Pederson, Reg. No. 38,269; and Nathan R. Rieth, Registration No. 44,302.

Please direct all telephone calls to Bruce R. Hopenfeld at (408) 433-8708 and all correspondence to:

LSI Logic Corporation  
Patent Law Department  
1551 McCarthy Boulevard, M/S D-106  
Milpitas, CA 95035

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I do hereby subscribe my name to the foregoing specification and claims, declaration, and power of attorney.

First Inventor's Full Name: Chintan Desai

Inventor's signature:  Date: 12/16/99

Residence: Sunnyvale, California

Citizenship: India

Post Office Address: 1049 W. Olive Avenue, #4, Sunnyvale, California 94086